

## EDUCATION

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**University of California, Santa Cruz**  
*PhD in CSE; GPA: 4.00/4.00; Advisor: Matthew Guthaus*

Santa Cruz, CA  
*September 2022 – Present*

**Ozyegin University**  
*BS in CS; GPA: 4.00/4.00*

Istanbul, Turkey  
*September 2017 – June 2022*

## RESEARCH

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**University of California, Santa Cruz**  
*PhD Student, Advisor: Prof. Matthew Guthaus*

Santa Cruz, CA  
*September 2022 – Present*

- **Gridless Router for OpenRAM:** OpenRAM is an open-source static random access memory (SRAM) compiler. OpenRAM's supply and signal router was a grid-based router, which had issues like DRC errors and bad precision due to pin-grid misalignment. I implemented a new router that created Hanan graphs over the routing region to align pins and wires perfectly. The new router is faster, more precise, DRC-safe, and uses less wire.

**Ozyegin University**  
*Research Intern, Advisor: Prof. H. Fatih Ugurdag*

Istanbul, Turkey  
*October 2020 – September 2021*

- **OpenCache:** An open-source generator to create custom caches using OpenRAM's SRAM arrays. It generates a synthesizable Verilog file for cache logic and configuration files for OpenRAM to generate the internal SRAMs of the cache. OpenCache inputs a configuration file that includes various parameters about the desired cache such as total size, number of ways, replacement policy, etc. Additionally, OpenCache can use other EDA tools to verify the output cache through randomly generated testbenches. This generator is written in Python using the Amaranth library, which is a Python-to-HDL toolkit.
- **Deep Compression for PyTorch Models:** Improving a "PyTorch to C generator" by applying compression methods on Convolutional Neural Networks (CNNs). Mr. Hasan Unlu of Tesla has developed a generator to deploy PyTorch models on microcontrollers efficiently. To improve this generator, I used pruning and quantization methods. Weights are saved as compressed sparse column (CSC) format to decrease memory usage and forward pass functions are improved to use CSC arrays directly without losing performance.

## EXPERIENCE

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**University of California, Santa Cruz**  
*Graduate Student Researcher*  
Worked on the OpenRAM project and research.

Santa Cruz, CA  
*January 2023 – Present*

**University of California, Santa Cruz**  
*Teaching Assistant*

Santa Cruz, CA  
*September 2022 – December 2022*

Assisted the following courses: Introduction to Data Structures and Algorithms (CSE101)

**Ozyegin University**  
*Undergraduate Teaching Assistant*

Istanbul, Turkey  
*September 2019 – June 2021*

Assisted the following courses: Computer Programming (CS101), Digital Systems (EE203), Computer Architecture (CS240)

## PROJECTS

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**Sobel Pipeline on FPGA**

Jan 2023 – Mar 2023

A sobel pipeline developed for the ASIC Systems Design course (CSE222) at the University of California, Santa Cruz. The pipeline is fed an image pixel by pixel and sobel filtered output is received the same way.

## PROGRAMMING SKILLS

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**Languages:** Python, C/C++, (System)Verilog, Chisel, Java, JavaScript, SQL, Bash

**Miscellaneous:** Git, Linux, Amaranth, PyTorch, Tensorflow